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of

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for

**BUFFERED RESIST PROFILE ETCH
OF A FIELD EMISSION DEVICE STRUCTURE**

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This is a continuation of U.S. Patent Application Serial No. 09/022,763, filed on February 12, 1998, entitled BUFFERED RESIST PROFILE ETCH OF A FIELD EMISSION DEVICE STRUCTURE, from which divisional U.S. Patent Application Serial No. 09/404,913 was filed on September 24, 1999, both of which are herein incorporated by reference in their entirety.

BACKGROUND OF THE INVENTION

The present invention relates to semiconductor structures for visual displays. More particularly, the present invention relates to a field emission device. In particular, the present invention relates to fabrication of a field emitter tip.

The Relevant Technology

Integrated circuits are currently manufactured by methods in which semiconductive structures, insulating structures, and electrically conductive structures are sequentially constructed in a predetermined arrangement on a semiconductor substrate. In the context of this document, the term "semiconductor substrate" is defined to mean any construction comprising semiconductive material, including but not limited to bulk semiconductive material such as a semiconductive wafer, either alone or in assemblies comprising other materials thereon, and semiconductive material layers, either alone or in assemblies comprising other materials. The term semiconductor substrate is contemplated to include such structures as silicon-on-insulator and silicon-on-sapphire. The term "substrate" refers to any supporting structure. As used herein, "field emission device" is defined to mean any construction for emitting electrons in the presence of an electrical field, including but not limited to an electron emission structure or tip either alone or in assemblies comprising other materials or structures.

Miniaturization of structures within integrated circuits focuses attention and effort to incorporating field emission devices within semiconductor substrates. A field emission

1 device typically includes an electron emission structure, or tip, configured for emitting a flux
2 of electrons upon application of an electric field to the field emission device. An array of
3 miniaturized field emission devices can be arranged on a plate and used for forming a visual
4 display on a display panel. For example, field emission devices may be used in making flat
5 panel displays for providing visual display for computers, telecommunication, and other
6 graphics applications. Flat panel displays typically have a greatly reduced thickness
7 compared to cathode ray tubes.

8 U.S. Patent No. 5,635,619 issued to Cloud et al. and U.S. Patent No. 5,229,331
9 issued to Doan et al. disclose field emission devices. The foregoing patents are hereby
10 incorporated by reference for purposes of disclosure. A general view of a field emission
11 device (FED) much like those that are disclosed in the foregoing patents to Cloud et al. and
12 Doan et al. particularly as geometries become relatively small, is seen in Figure 1. The FED
13 employs a cold cathode and includes a substrate 28, which can be composed of glass, for
14 example, or any of a variety of other suitable materials. A cathode conductive layer 30, such
15 as doped polycrystalline silicon, is deposited onto substrate 28.

16 At a field emission site location, an emitter tip 14, which is a micro-cathode, is
17 constructed over substrate 28. A variety of shapes have been used for emitter tip 14, so long
18 as the emitter tip 14 tapers to a relatively fine point. Surrounding emitter tip 14 is a low
19 potential anode gate structure 38, which is separated from cathode conductive layer 30 by
20 means of a dielectric layer 34.

21 When a voltage differential is applied between emitter tip 14 and anode gate
22 structure 38 using, for example, voltage source 32, an electron flux 24 is emitted and
23 accelerates toward an anode panel 26. The anode panel 26 includes a transparent panel 44,
24 such as glass; a phospholuminescent panel 48; and an anode conductive layer 46, which is
25 electrically connected to source 32. The electron flux 24 strikes and excites the
26 phospholuminescent panel 48, thereby causing light 36 to be emitted and to pass through

1 transparent panel 44.

2 The coordinated activity of a plurality of emitter tips 14 arrayed over a flat panel
3 display provides a visual display that may be viewed by a user. Each individual or cluster
4 of emitter tips 14 that is provided on a flat panel display may be assigned a unique matrix
5 address. When such a flat panel display is used, the emitter tips 14 are systematically
6 activated by means of their matrix addresses in order to provide the desired visual display.

7 Significant problems with emitter tip 14 in the above described device are evident
8 in the prior art due to shrinking geometries. As seen in Figure 1, manufacturing processes
9 that are commonly used in the prior art typically form an emitter tip 14 that has a curvilinear
10 vertical profile. Figure 2 illustrates an intermediate stage in the formation of emitter tip and
11 further depicts the curvilinear vertical profile thereof. In Figure 2, the intermediate
12 semiconductor structure 10 comprises cathode conductive layer 30, emitter tip 14, and a hard
13 mask 16 that covers emitter tip 14 prior to its removal. It can be seen that emitter tip 14
14 includes wings 18 that cause the vertical profile of emitter tip 14 to be curvilinear instead of
15 rectilinear. Wings 18 are unintentional but persistent products of conventional methods of
16 forming emitter tip 14. Emitter tips 14 that have pronounced curvilinear vertical profiles
17 have been found to provide sub-grade performance compared to those that are more nearly
18 rectilinear.

19 Emitter tip 14 is exposed to the etch gas at large, but it encounters two types of etch
20 gas molecules. A primary collision etch gas molecule 8 (its trajectory illustrated) collides
21 with emitter tip 14 by coming from the etch gas at large. A secondary collision etch gas
22 molecule 12 (its trajectory illustrated) comes from the etch gas at large but it collides with
23 and rebounds from hard mask 16 near the intersection of emitter tip 14 and hard mask 16 just
24 prior to its etch collision with emitter tip 14. Because the etch is selective to hard mask 16,
25 the secondary collision etch gas molecule 12 rebounds from hard mask 16 and, along with
26 primary collision etch gas molecule 8, causes an intensified frequency of collisions into

1 emitter tip 14 in the region of the intersection between hard mask 16 and emitter tip 14. The
2 intensified frequency of collisions into emitter tip 14 by secondary collision etch gas
3 molecule 12 in addition to primary collision etch gas molecule causes increased etching of
4 emitter tip 14 in this region. The increased etching in this region is exacerbated by the
5 increase in surface area that is formed due to both primary- and secondary-collision etch gas
6 molecules. Further, the extinguishment of secondary etch gas molecule 12 causes an etch
7 gas sink which intensifies etching in this region. Hence, wings 18 form because of
8 intensified etching activity in the region of emitter tip 14 near hard mask 16.

9 As geometries continue to shrink to the point that the mean free path of secondary
10 etch gas molecule 12 is greater than the distance from its collision point on hard mask 16 to
11 emitter tip 14, the problem is only made more pronounced. Additionally, as wings 18 begin
12 to form against hard mask 16, the surface area of emitter tip 14 above wings 18 increases.
13 The increased surface area makes for increased primary and secondary etch gas molecules
14 that collide with emitter tip 14 in this region. This increases etching in this region as
15 compared to the region below wings 18.

16 In the prior art, hard mask 16 was formed by patterning a photoresist upon an oxide
17 layer, etching to form hard mask 16, and stripping the photoresist. Problems of a curvilinear
18 profile arose in part from etching difficulties as emitter tip geometries continued to shrink.
19 Achieving a substantially rectilinear profile became more elusive as geometries shrank and
20 it became more and more challenging to get an undercutting etch beneath hard mask 16 so
21 as to yield an emitter tip having a rectilinear profile. Because an undercutting etch is a
22 preferred method of achieving emitter tip 14, what is needed in the art is a method of forming
23 a substantially rectilinear profile of an emitter tip as geometries continue to shrink.
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SUMMARY OF THE INVENTION

The present invention relates to formation of an emitter tip that overcomes the problems in the prior art. A substrate is provided, and a cathode conductive layer is formed thereupon. An emitter layer is formed on the resistive layer. The emitter layer may be any material from which electron emission structures may be formed, especially those materials having a relatively low work function, so that a low applied voltage will induce a relatively high electron flux therefrom. An emitter tip is formed according to the inventive method. In a first procedure, the emitter layer is overlaid with a blanket dielectric which is in turn overlaid by a masking layer and patterned into a masking island according to a size that is dictated by dimensions of the emitter tip to be formed.

In a first etching stage, the masking island is used to etch substantially anisotropically into the oxide to form the oxide island that has substantially the same "footprint" as the masking island.

In a second etching stage, the emitter layer is etched with an etch recipe that is selective to the underlying structure which is positioned beneath the emitter layer. Selectivity of the second etching stage recipe to the masking island is not as great as the selectivity thereof to the oxide island and to the underlying structure. The characteristics of this second etching stage are such that both isotropic and anisotropic qualities are exhibited in the etch recipe. By this combination of qualities, both penetration through the emitter layer and undercutting beneath the oxide island are achieved. In a preferred embodiment, the second etching stage is carried out under etching conditions with the following preferred etching characteristics. Firstly, the directional qualities of the second etching stage etch recipe, as set forth above, include both isotropic and anisotropic characteristics. Secondly, partial mobilization of the masking island creates a skirt region that substantially alters the etch gas that it encounters.

1 In a third etching stage, selectivity of the etch recipe to the masking island is
2 configured to be lower than in the second etching stage. Additionally, the third etching stage
3 is carried out under conditions that are substantially more anisotropic than in the second
4 etching stage.

5 An advantage of the inventive method over the prior art is that the masking island
6 does not need to be removed during the inventive etching stages. Additionally according to
7 the present invention, selection of an application-specific chemistry for the masking island
8 prepares the emitter layer for the buffered etching of the second and third etching stages that
9 provide another advantage of a more rectilinear etched profile of the emitter tip.

10 The present invention has application to a wide variety of field emission devices
11 other than those specifically described herein. In particular, achievement of the emitter tip
12 with a substantially rectilinear profile increases the efficiency of electron emission and
13 therefore lowers the power and increases the ability to achieve higher refresh rates for a video
14 display application.

15 These and other features of the present invention will become more fully apparent
16 from the following description and appended claims, or may be learned by the practice of the
17 invention as set forth hereinafter.

BRIEF DESCRIPTION OF THE DRAWINGS

In order that the manner in which the above-recited and other advantages of the invention are obtained, a more particular description of the invention briefly described above will be rendered by reference to specific embodiments thereof which are illustrated in the appended drawings. Understanding that these drawings depict only typical embodiments of the invention and are not therefore to be considered to be limiting of its scope, the invention will be described and explained with additional specificity and detail through the use of the accompanying drawings in which:

Figure 1 is a prior art cross-sectional elevation view of a conventional field emission device, whereby it can be seen that an emitter tip has a substantially curvilinear vertical profile due to increasing etch difficulties that are encountered as geometries continue to shrink.

Figure 2 is a elevational cross-section view of an emitter tip in an intermediate processing stage according to the problem depicted in the prior art, wherein it can be seen that the emitter tip has a swollen or winged portion.

Figure 3 is an elevational cross-section view of a precursor structure for forming an emitter tip according to the present invention, wherein an emitter layer is formed over a substrate and wherein a blanket dielectric layer and a masking layer are successively formed over the emitter layer.

Figure 4 is an elevational cross-section view of the structure depicted in Figure 3 after further processing, wherein an oxide island has been formed upon the emitter layer by patterning the masking layer and subsequently etching a portion of the blanket dielectric layer.

Figure 5 is an elevational cross-section view of the structure depicted in Figure 4 according to the present invention after further processing, wherein both isotropic and anisotropic etching is carried out to form a substantially rectilinear vertical etched profile of

1 the emitter tip, wherein at least a portion of the masking island material is mobilized to
2 protect and buffer the oxide island.

3 Figure 6 is an elevational cross-section view of an emitter tip according to an
4 embodiment achieved by the inventive method, wherein it can be seen that the emitter tip has
5 a substantially paraboloid vertical profile that arcs in a concave fashion or of a section of a
6 geometric oval fashion. The concave or oval section shape extends between a substrate
7 below the emitter tip and a hard mask at the apex of the emitter tip.

8 Figure 7 is an elevational cross-section view of the structure depicted in Figure 5
9 after further processing, wherein a completed field emission device is provided and includes
10 an emitter tip formed according to the invention.

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1 **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**

2 The present invention relates to a method of forming an FED that overcomes the
3 problems of the prior art. In particular, the present invention includes a method for
4 constructing a cathode structure in the form of a conical, tapered emitter tip for use in a field
5 emission device. Reference will now be made to the drawings wherein like structures will
6 be provided with like reference designations. It is to be understood that the drawings are
7 diagrammatic and schematic representations of the embodiment of the present invention and
8 are not drawn to scale.

9 In practice, emitter tips are typically formed in physical relationship with a number
10 of other structures that together form a field emission device. Multiple field emission
11 devices may be arranged to form a flat panel display or other visual display device.
12 However, the methods disclosed herein are generally applicable to the formation of
13 substantially any emitter tip that is to have a tapered structure and a substantially rectilinear
14 vertical profile, regardless of the other particular features of the field emission device or
15 other structure in which it is to be used. Accordingly, although examples are disclosed
16 hereinafter of specific field emission devices that include an emitter tip formed according to
17 the methods of the invention, it is to be understood that the invention is generally applicable
18 to forming emitter tips that may be used in a wide variety of field emission devices.

19 Figure 3 illustrates a multi-layer structure 50 having undergone several initial steps
20 in the process of forming an FED according to a preferred embodiment of the invention. A
21 substrate is provided, and is preferably a P-type silicon wafer having formed therein (by
22 suitable known doping pretreatment) a series of elongated, parallel extending opposite N-
23 type conductivity regions, or wells. Each N-type conductivity strip has a width of
24 approximately 10 microns, and depth of approximately 3 microns. The spacing of the strips
25 is arbitrary and can be adjusted to accommodate a desired number of field emission cathode
26 sites to be formed on a given size silicon wafer substrate.

1 Processing of the substrate to provide the P-type and N-type conductivity regions
2 may be by any suitable semiconductor processing techniques, such as diffusion and/or
3 epitaxial growth. If desired, the P-type and N-type regions, of course, can be reversed
4 through the use of a suitable starting substrate and appropriate dopants.

5 The N-type or P-type conductivity strips, or wells, are to be the sites at which emitter
6 tips are to be formed. As such, each conductivity strip constitutes a emitter layer 62, from
7 which material is to be selectively removed in order to construct emitter tips. It will be
8 understood that an emitter layer 62 may be provided upon a substrate according to alternative
9 procedures other than the above-described process of forming doped wells or strips within
10 the substrate. For example, a conformal layer of doped polysilicon may be deposited or
11 otherwise formed over a substrate in order to provide an emitter layer 62 from which an
12 emitter tip is to be constructed.

13 Regardless of the preliminary steps conducted to provide emitter layer 62, the
14 method of forming an emitter tip therefrom is illustrated in Figures 3-6 and is described
15 hereinafter. In a first procedure seen in Figure 3, emitter layer 62 is overlaid with a blanket
16 dielectric 56 such as, by way of non-limiting example, an oxide. The oxide is overlaid by
17 a masking layer 58 and patterned into a masking island 68 as seen in Figure 4 according to
18 a size that is dictated by the desired dimensions of emitter tip that is to be formed.

19 In a first etching stage, masking island 68 is used to etch substantially anisotropically
20 into the oxide to form oxide island 66 that has substantially the same "footprint" as masking
21 island 68 as seen in Figure 4. The etch to form oxide island 66 is highly selective to masking
22 island 68 and is also configured to stop on emitter layer 62. By way of non-limiting example,
23 oxide island 66 is formed by an oxide dry etch. In this way, oxide island 66 is formed
24 according to specifications.

25 In a second etching stage, emitter layer 62 is etched with an etch recipe that is
26 selective to the structure beneath emitter layer 62, where a discrete structure is to provide a

1 base upon which an emitter tip will rest. In this example, the discrete structure comprises
2 underlying structure 60, which may be a portion of a polysilicon substrate that is doped
3 differently than emitter layer 62. Selectivity of the second etching stage recipe to masking
4 island 68 is not as great as the selectivity thereof to oxide island 66 and to underlying
5 structure 60.

6 The characteristics of this second etching stage are such that both isotropic and
7 anisotropic qualities are exhibited in the etch recipe. By this combination of qualities, both
8 penetration through emitter layer 62 and undercutting beneath oxide island 66 are achieved.
9 Additionally, the second etching stage is not as selective to masking island 68 as is the first
10 etching stage. This causes masking island 68 to begin to become mobilized at this second
11 etching stage.

12 The etch chemistry may be selected to a preferred single etch gas under conditions
13 that achieve both isotropic and anisotropic etch qualities. Alternatively, a mixture of etch
14 gases may be selected along with other etch conditions such that a gas that etches
15 isotropically is mixed with a major amount of a gas that etches anisotropically. Selection of
16 conditions, whether with a single gas or with a gas mixture will depend upon the specific
17 application. The specific application will depend upon the chemical makeup of the structures
18 that are being removed and those that are to act as etch stops.

19 By way of nonlimiting example, the second etching stage is carried out under plasma
20 enhanced etching conditions. Where a plasma is generated during an etch, etch temperatures
21 may be carried out in a lower range than otherwise. Under these conditions, temperatures
22 are sufficiently low so as to not substantially volatilize masking island 68.

23 Figure 5 depicts formation of emitter tip 64 at a point that is during the second
24 etching stage. A fraction of masking island 68 has become mobilized by as seen by a slight
25 tapering thereof. Although no single theory is relied upon, mobilization of a fraction of
26 masking island 68 apparently causes the mobilized portion to act as a buffer to the etch gas

1 or etch gases. Control of the buffering effect of a partial mobilization of masking island 68,
2 in addition to selection of an etch gas or to selection of a mixture of etch gases, may be
3 affected positively by selecting the step height 70 of masking island 68. Where a higher step
4 height 70 is formed, an increased surface area will be available to be mobilized during the
5 second etching stage.

6 In a preferred embodiment of the present invention, the second etching stage is
7 carried out under etching conditions with the following preferred etching characteristics.
8 Firstly, the directional qualities of the second etching stage etch recipe, as set forth above,
9 include both isotropic and anisotropic characteristics. Secondly, partial mobilization of
10 masking island 68 creates a skirt region 108, that substantially alters the etch gas, and that
11 extends downwardly from the upper surface 100 and the lateral edge 102 of oxide island 66.
12 Skirt region 108 of the substantially altered etching gas extends downwardly toward the
13 receding surface 104 of emitter layer 62.

14 As lateral diffusion of etching gas through skirt region 108 occurs, the etching gas
15 is substantially altered so as to be highly selective to oxide island 66 but the etching gas
16 retains isotropic etching characteristics that continue to cause a substantially rectilinear
17 etched profile of emitter tip 64. By such etching characteristics caused by mobilization of
18 masking island 68 and its protection of oxide island 66 during the second etching stage, a
19 substantially conical shape is achieved in emitter tip 64. From a point T at the top of emitter
20 tip 64 to a point β at the base of emitter tip 64, a line can be drawn that makes a particular
21 angle α , as seen in Figure 5. The angle α is measured from an axis perpendicular to the
22 general plane formed of emitter layer 62 and is preferred to be in a range from about 20
23 degrees to about 60 degrees. More preferably, the angle is in a range from about 25 degrees
24 to about 40 degrees, and most preferably about 25 degrees to about 30 degrees.

25 In a third etching stage, selectivity of the etch recipe to masking island 68 is
26 configured to be lower than in the second etching stage. Additionally, the third etching stage

1 is carried out under conditions that are substantially more anisotropic than in the second
2 etching stage. Where underlying structure 60 is present, an etch recipe is configured to stop
3 on underlying structure 60, but that will mobilize a portion of masking island 68 to a greater
4 degree than mobilization thereof that is achieved in the second etching stage.

5 In this third etching stage, it is useful to protect masking island 68 from etching after
6 a manner that allows for continued undercutting beneath masking island 68 while
7 simultaneously protecting masking island 68 by the buffering effect thereon of a partially
8 mobilized masking island 68. Where underlying structure 60 is not present, etching
9 conditions are selected to stop etching when a preferred height of emitter tip 64 has been
10 achieved.

11 During the third etching stage, about two-thirds of the height of emitter tip 64 is
12 achieved by removing substantially all of the remainder of emitter layer 62 down to stop on
13 underlying structure 60 if underlying structure 60 is present. In Figure 5, it can be seen that
14 a second etching stage tip profile height 72 has exposed emitter tip 64 to a level above
15 underlying structure 60. A third etching stage tip profile height 74 is also illustrated as an
16 alternative target profile height. Whether underlying structure 60 is present or not, whether
17 any or all structures beneath emitter layer 62 are present or not, or whether it is desirable or
18 not to leave at least a portion of emitter layer 62 as illustrated in Figure 5, the third etching
19 stage is carried out in which about two thirds of the final height of emitter tip 64 is formed.

20 An advantage of the inventive method over the prior art is the selection of masking
21 island 68 that does not need to be removed during the inventive etching stages. By retaining
22 the photoresist of masking island 68, if masking island 68 is composed of photoresist,
23 additional steps of stripping masking island 68 and a series of cleans are eliminated.

24 Additionally according to the present invention, selection of an application-specific
25 chemistry for masking island 68 prepares emitter layer 62 for the buffered etching of the
26

1 second and third etching stages that provide another advantage of a more rectilinear etched
2 profile of emitter tip 64.

3 At the substantial completion of the third etching stage, where masking island 68
4 comprises a positive photoresist of a novalac resin and a photosensitizer, masking island 68
5 has been attrited by about one-fourth its original mass. While no single theory is to be relied
6 upon, it is considered useful to assume that the mobilized masking island 68 substantially
7 diminishes the effect of the etch recipe of the third etching stage to remove substantially any
8 of oxide island 66 in the region of the undercut such that a substantially rectilinear emitter
9 tip profile is formed.

10 Figure 6 illustrates one achieved embodiment of the present invention according to
11 the inventive method following completion of the third etching stage. For illustrative
12 purposes, the vertical profile of emitter tip 64 is exaggerated to illustrate a deviation from
13 absolute rectilinearity. In Figure 6 it can be seen that emitter tip 64 has an emitter tip profile
14 106 that has an arc length L and a chord length C. Emitter tip 64 has a height H and emitter
15 tip profile 106 has a parabolic or oval sectional shape that subtends from the linearity of
16 chord length C by a depth D. Emitter tip 64, formed by the method of the present invention,
17 avoids the formation of wings 18 as illustrated in the prior art by having a substantially
18 rectilinear profile. The example of Figure 6 is presented to illustrate an example of
19 substantial rectilinearity under the invention when the vertical profile of emitter tip deviates
20 from absolute rectilinearity.

21 Under substantially ideal conditions, arc length L and chord length C are
22 substantially the same. Under substantially ideal conditions, the subtending of emitter tip
23 profile 106 away from chord length C will deviate by a depth of about $D = 0$. In a preferred
24 embodiment of the present invention the ratio of arc length L over chord length C is less than
25 or equal to about 1.2:1. More preferably, the ratio of arc length L to chord length C is less
26 than or equal to about 1.1:1. Even more preferably the ratio of arc length L to chord length

1 C is less than or equal to about 1.05:1. Most preferably, the ratio of arc length L over chord
2 length C is less than or equal to about 1.01:1.

3 According to the method of the present invention, as emitter tip 64 is formed in the
4 second etching stage and the third etching stage, the buffering effect caused by mobilization
5 of masking island 68 tends to diminish the isotropic etching effects of the second etching
6 stage in regions of emitter tip 64 near oxide island 66. As etching away from oxide
7 island 66 in the direction of underlying structure 60 is carried out, the buffering effects of
8 mobilized masking island 68 is reduced.

9 In the inventive method, secondary collision etch gas molecules are substantially
10 reduced. The reduction of secondary collision etch gas molecules 12 may be caused by such
11 molecules being chemically neutralized as they collide with molecules from the mobilized
12 portions of masking island 66. The reduction of secondary collision etch gas molecules 12
13 may also be caused by would-be secondary collision etch gas molecules 12 that transfer their
14 momentum to molecules of mobilized portions of masking island in skirt region 108.

15 Following formation of emitter tip 64, further processing may be carried out in order
16 to construct, in the vicinity of emitter tip 64, structures that enable an electric field to be
17 applied to emitter tip 64 such that an electron flux is emitted therefrom. It will be understood
18 that any of a number of structures and corresponding processes may be used according to the
19 invention to form the aforementioned structures in the vicinity of emitter tip 64. For
20 example, Figure 7 illustrates a partial cross section of a completed flat panel display that
21 includes emitter tip 64 as part of a field emission device. It may be noted that the structure
22 of Figure 7 is substantially similar in many aspects to the structure of Figure 1, with the
23 marked difference of the substantial rectilinearity of emitter tip 64 of Figure 7, which is a
24 result of the inventive method.

25 Accordingly, an advantageous method that may be used to construct a completed
26 field emission device after emitter tip 64 has been formed is described in U.S. Patent Nos.

1 5,653,619 and 5,229,331. In particular, such methods result in a field emission device that
2 includes a dielectric layer 76 that separates, physically and electrically, a conductive gate
3 structure 78 from cathode conductive layer 80. An anode panel 90 is positioned over
4 conductive gate structure 78 and is separated therefrom by a substantial vacuum 82. Anode
5 panel 90 includes a transparent panel 92, an anode conductive layer 94, and a
6 phospholuminescent panel 96.

7 While as few as one emitter tip 64 may be formed, in practice, it is common to form
8 an array of as many as tens of millions or more of emitter tips 64 over a substrate. The
9 formation of emitter tip 64 as illustrated in Figure 6 and 7, such that wings have been
10 avoided and emitter tip 64 has a substantially rectilinear vertical profile, provides a geometry
11 that is highly efficient for generating an electron flux. In particular, the localized work
12 function of the material that constitutes emitter tip 64 is relatively low at the apex of the
13 emitter tip 64. As a result, a relatively high electron flux 86 can be generated from a given
14 voltage, and electron emission will be substantially limited to the apex.

15 For the purpose of achieving a substantially rectilinear profile for emitter tip 64, it
16 should first be recognized that economic considerations encourage manufacturing processes
17 that have high product throughput. The present invention provides distinct advantages over
18 the prior art in decreasing processing time and costs. By the methods of the prior art, several
19 steps were required to prepare hard mask 16 for an etching process that formed emitter tip
20 14. Patterning of hard mask 16 was required by use of a photoresist. Following formation
21 of the hard mask, several steps of photoresist removal and cleaning were required.

22 One advantage of the present invention over the prior art is selection of a preferred
23 material to form masking island 68 whereby oxide island 66 is formed but that
24 simultaneously provides a preferred processing path that avoids the need to strip masking
25 island 68 and several subsequent steps of cleaning multilayer structure 50. Thus, masking
26 island 68 is first used as a masking means in the formation of oxide island 66. According

1 to the inventive method, masking island 68 is next used as a buffering means to assist during
2 the second etching stage and the third etching stage to achieve emitter tip 64 that has a
3 substantially rectilinear profile.

4 Where third stage tip profile height 74 may be higher than previous applications,
5 mask step height 70 may be increased to provide additional surface area of masking island
6 68 that can be mobilized to act as a buffer medium during the second etching stage and the
7 third etching stage. Where third stage tip profile height 74 is shorter than that achieved
8 previously, such as during a miniaturization effort, mask step height 70 may be decreased,
9 thus providing a smaller surface area of masking island 68 that can be mobilized during the
10 formation of emitter tip 64. Thus, the process engineer may select processing conditions to
11 achieve a preferred degree of mobilization of the photoresist making up masking island 68.

12 A field emission device that includes emitter tip 64 formed according to the
13 invention may be used in the customary manner to produce visible light. In particular emitter
14 tip 64 and an associated field emission device are used by applying voltages to cathode
15 conductive layer 80, conductive gate structure 78 and anode conductive layer 94 by means
16 of voltage source 98. Preferably, the voltage applied to conductive gate structure 78 is
17 positive with respect to the voltage applied to cathode conductive layer 80. The voltage
18 applied to anode conductive layer 94 should also be positive, but with a significantly greater
19 magnitude than that of conductive gate structure 78. This significantly higher voltage causes
20 electrons emitted from emitter tip 64 to be accelerated toward anode panel 90 such that they
21 strike phospholuminescent panel 96. Electron flux 86 excites the material of
22 phospholuminescent panel 96 such that visible light is emitted therefrom.

23 The present invention has application to a wide variety of field emission devices
24 other than those specifically described herein. In particular, achievement of emitter tip 64
25 with a substantially rectilinear profile increases the efficiency of electron emission and
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1 therefore lowers the power and increases the ability to achieve higher refresh rates for a video
2 display application.

3 The present invention may be embodied in other specific forms without departing
4 from its spirit or essential characteristics. The described embodiments are to be considered
5 in all respects only as illustrated and not restrictive. The scope of the invention is, therefore,
6 indicated by the appended claims and their combination in whole or in part rather than by the
7 foregoing description. All changes that come within the meaning and range of equivalency
8 of the claims are to be embraced within their scope.

9 What is claimed and desired to be secured by United States Letters Patent is:

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